What is claimed is:

1. A method of writing to a synchronous non-volatile memory device comprising:

receiving write data on a first clock cycle and executing a data write operation; and

executing a data read operation on a next clock cycle immediately following the first clock cycle.

2. The method of claim 1 wherein the data write operation is executed on a first memory bank of the synchronous non-volatile memory device and the data read operation is executed on a second memory bank.

3. The method of claim 1 further comprising latching the write data on the first clock cycle.

4. The method of claim 1 wherein executing the data write operation comprises:

receiving a write command;

receiving a row address; and

receiving a column address, wherein the column address is received on the first clock cycle in synchronization with the write data.

5. The method of claim 1 further comprises:

latching the write data in a write latch on the first clock cycle; and

performing a write operation during the next clock cycle to store the write data in the synchronous non-volatile memory device.

6. A method of operating a synchronous memory device comprising:

receiving write data on data connections;

latching the write data in a write latch;

releasing the data connections after the write data is latched; and

performing a read operation on the synchronous memory device while the write data is transferred from the write latch to memory cells.

7. The method of claim 6 wherein the read operation is initiated in response to a read command received by the synchronous memory device on a second clock cycle immediately following a first clock cycle coincident with receiving the write data.

8. The method of claim 6 further comprises:

receiving a row address on a first clock cycle;

receiving a column address on a second clock signal following the first clock signal, wherein the write data is received on the data connections on the second clock cycle.

9. The method of claim 8 wherein the read operation is initiated in response to a read command received by the synchronous memory device on a third clock cycle immediately following a second clock cycle.

10. The method of claim 6 wherein the synchronous memory device comprises an array of non-volatile memory cells.

11. A method of writing to a synchronous memory device comprising:

providing a write command and write data from a processor to the synchronous memory device on a first clock cycle;

storing the write data in a write latch of the synchronous memory device; and

performing a write operation to copy the write data from the write latch to a memory array of the synchronous memory device; and

providing a read command from the processor to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a read operation on the memory array.

12. The method of claim 11 wherein the write data is copied to a first bank of the memory array and the read operation is performed on a second bank of the memory array.

13. The method of claim 11 wherein the processor provides a row address, and a column address, wherein the column address is provided on the first clock cycle in synchronization with the write data.

14. A synchronous memory device comprising:

a memory array arranged in rows and columns;

data communication connections for bi-directional data communication with an external device;

data buffer coupled to the data communication connections to manage the bi-directional data communication; and

a write latch coupled between the data buffer and the memory array to latch data provided on the data communication connections.

15. The synchronous memory device of claim 14 further comprising control circuitry to copy the data from the write latch to the memory array.

16. The synchronous memory device of claim 15 wherein the memory array is arranged in a plurality of memory blocks, and the control circuitry is configured to copy the data from the write latch to a first block of the plurality of the plurality of memory blocks.

17. The synchronous memory device of claim 16 wherein the control circuitry is further configured to read data from a second block of the plurality of memory blocks while the data is copied to the first block.

18. The synchronous memory device of claim 14 wherein the memory array comprises non-volatile memory cells.

19. A method of operating a synchronous memory device comprising:

receiving a read command and corresponding column address on a first clock cycle to request output data from a memory array of the synchronous memory, wherein the output data is provided on an external data connection a predefined number of clock cycles following the first clock cycle; and

receiving a first command of a write command sequence on a second clock cycle immediately following the first clock cycle to initiate a write operation to the memory array such that the write command is provided in coincidence with or prior to providing the output data on the external data connection.

20. The method of claim 19 wherein the write command sequence comprises:

a load command register cycle used to initiate the write operation;

an active cycle used to define and activate a selected row of the memory array; and

a write cycle used to define a column of the memory array and provide write data on the external data connection.

21. The method of claim 19 wherein the memory array comprises non-volatile memory cells.

22. A method of initiating a write operation in a memory system, the method comprises:

providing a read command from a processor to a synchronous memory device;

providing a memory array address from the processor to the synchronous memory device on a first clock cycle of a memory array location to perform a read operation;

providing a first command of a write command sequence from the processor to the synchronous memory device on a second clock cycle immediately following the first clock cycle to initiate a write operation of the memory array such that the write command is provided prior to providing output data from the memory array address on an external data connection.

23. The method of claim 22 wherein the write command sequence comprises:

a load command register cycle used to initiate the write operation;

an active cycle used to define and activate a selected row of the memory array; and

a write cycle used to define a column of the memory array and provide write data on the external data connection.

24. A memory system comprising:

a processor; and

a synchronous memory device coupled to the processor via a bi-directional data bus, the synchronous memory device comprises,

a memory array arranged in rows and columns;

data communication connections coupled to the bi-directional data bus;

an input/output data buffer coupled to the data communication connections to manage bi-directional data communication; and

a write latch coupled between the data buffer and the memory array to latch data provided on the data communication connections.

25. The memory system of claim 24 wherein the memory array is arranged in a plurality of memory blocks, and the synchronous memory comprises control circuitry configured to copy the data from the write latch to a first block of the plurality of the plurality of memory blocks.

26. The memory system of claim 25 wherein the control circuitry is further configured to read data from a second block of the plurality of memory blocks while the data is copied to the first block.

27. The memory system of claim 24 wherein the memory array comprises non-volatile memory cells.